## **CLAIMS**

1. An integrated circuit memory including:

at least two banks, each of which is provided with an array of storage elements having at least one redundancy column and is associated with specific sense amplifiers;

a row of input/output buffer circuits common to the memory banks; and

for each memory bank, a circuit for assigning the redundancy column to an input/output line connected to one of said buffers, the assigning being performable, for a line of current rank, towards the columns of preceding rank and towards the columns of following rank;

wherein each assignment circuit associated with a memory bank includes means for branching the input/output lines and conductors of individual activation of the sense amplifiers of the involved memory bank.

- 2. The memory of claim 1, wherein said assignment circuits are switches for branching input/output lines formed in a same metallization level.
  - 3. The memory of claim 2, wherein the input/output lines and the conductors of activation of the sense amplifiers are formed in a same metallization level, said lines and said conductors being interrupted at the level of each assignment circuit.

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- 4. The memory of claim 1, wherein the sense amplifiers are arranged in rows perpendicular to the columns.
- 5. The memory of claim 1, wherein the number of sense amplifiers per bank corresponds to the total number of columns of the arrays of storage elements, the number of input/output buffers corresponding to the number of columns of storage elements outside of the redundancy column.
  - 6. The memory of claim 1, wherein the assignment circuits are programmed by means of non-volatile memory registers.

7. The memory of claim 1, including means for individually addressing each assignment circuit.